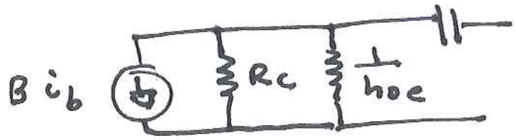
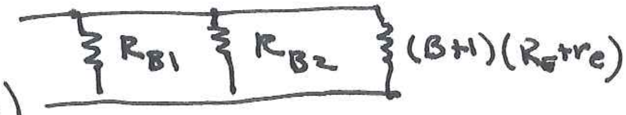
Build this circuit!

AC as viewed from collector



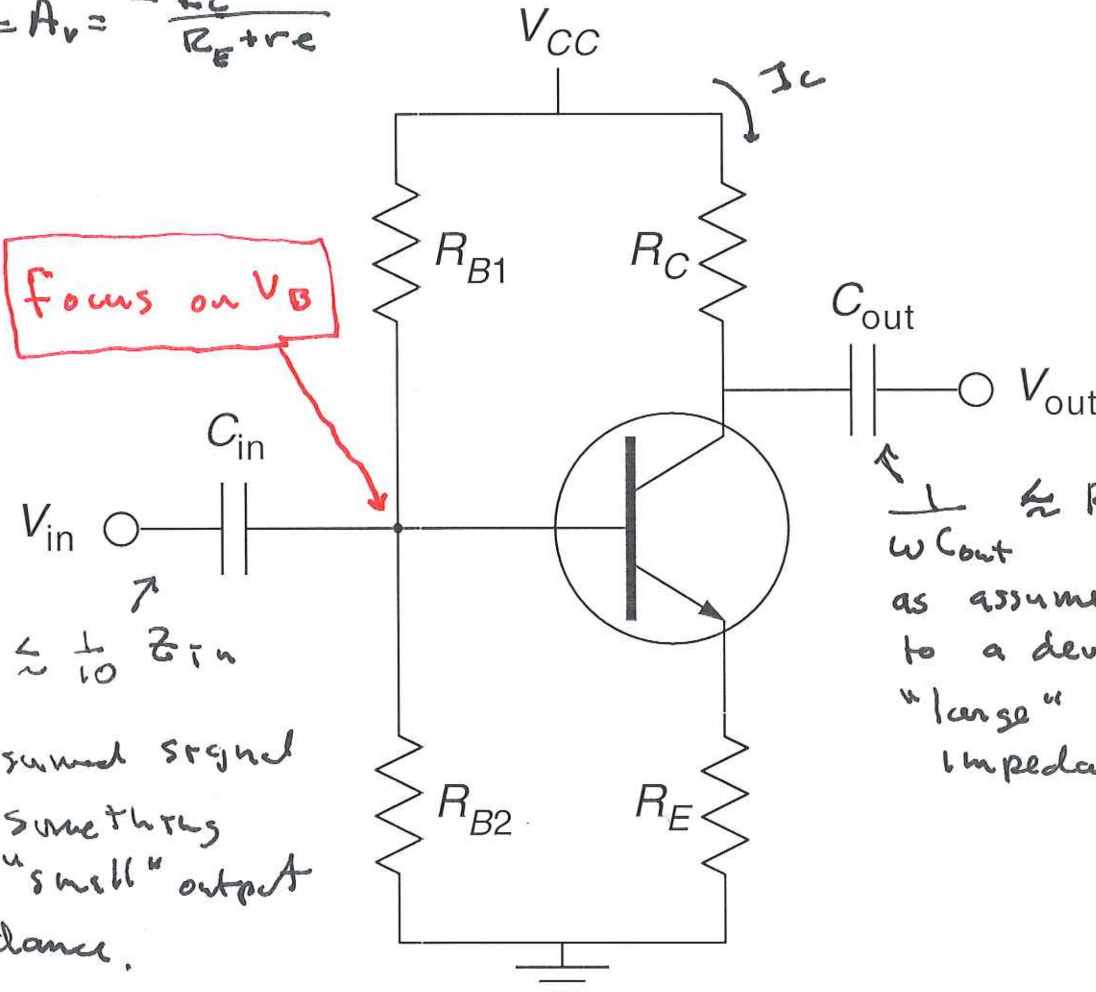

$$Z_{out} = R_C \parallel \frac{1}{h_{oe}} \approx R_C$$

AC as viewed from base




$$Z_{in} = R_{B1} \parallel R_{B2} \parallel (B+1)(R_E+r_e)$$

$$\text{Gain} = A_v = \frac{-R_C}{R_E + r_e}$$




$\frac{1}{\omega C_{out}} \lessapprox R_C$ as assumed connected to a device with "large" input impedance

$\frac{1}{\omega C_{in}} \lessapprox \frac{1}{10} Z_{in}$ as assumed signal from something with "small" output impedance.

Design: $V_{CE} = \frac{1}{2} V_{CC} \Rightarrow \frac{1}{2} V_{CC}$ divided between $R_C$ & $R_E$

$$I_E = \frac{\frac{1}{2} V_{CC}}{R_E + R_C}$$

$$V_E = \frac{1}{2} V_{CC} \frac{R_E}{R_E + R_C} = \frac{1}{2} V_{CC} \frac{1}{1 + |A_v|}$$

Now: $$\frac{\Delta V_{CE}}{V_{CE}} = \frac{-\Delta I_E (R_E + R_C)}{V_{CC}/2} = -\frac{\Delta I_E}{I_E} = -\frac{\Delta V_E}{V_E}$$ ← circumstances inside BJT [Temp, $V_{CE}$] can change this by ±.1V

to assure accurately set — use large $V_E$ ... 1V?, $\frac{1}{3} V_{CC}$?, $\frac{1}{20} V_{CC}$?

It would be nice if this were "small" but that turns out to be hard to do

Design: decide on $Z_{out}$ ($R_C$) & gain $= A_v$

$"R_E" = \frac{R_C}{|A_v|}$ ← this neglects $r_e$; if desired correct with $R_E \leftarrow "R_E" - r_e$

min freq & $R_C \Rightarrow C_{out}$

$I_C = \frac{V_{cc}/2}{(R_C + R_E)}$ → calculate $r_e = \frac{25}{I_C}$ ← really should be $I_E$

use $I_C$

Main point: $V_E = R_E I_E$ → $V_B = V_E + .6$
judge $\beta$ → $I_B = \frac{I_C}{\beta}$
] design $R_{B1}, R_{B2}$ "bias"

Method 1: Design a "stiff" voltage divider with
$R_{TH} <<$ "impedance looking in base" $= (\beta+1)(r_e + R_E)$

$R_{B1} || R_{B2}$

$\frac{V_B}{V_{cc}} = \frac{R_{B1} || R_{B2}}{R_{B1}}$ ] solve for $R_{B1}$ then $\frac{1}{R_{B2}} = \frac{1}{R_{B1} || R_{B2}} - \frac{1}{R_{B1}}$

Note: because of voltage droop the actual $V_B$ will be smaller than design → $V_E$ small → $V_{CE}$ big. Only if $\beta = \infty$ (i.e. $I_B = 0$) will design match reality

Method 2: Having guessed a $\beta$ (& hence $I_B$) use it, but make sure there is "lots" of extra current available →

$I_{B1} = \frac{(V_{cc} - V_B)}{R_{B1}} = 10\, I_B$ [solve $R_{B1}$]

$I_{B2} = \frac{(V_B - 0)}{R_{B2}} = 9\, I_B$ [solve $R_{B2}$]

Note: in this case if $\beta = \infty$ ($r_e I_B = 0$), $V_B$ will be larger than design (cuz we built in the droop) → larger $V_E$ → smaller $V_{CE}$

Example: $V_{CC} = 15V$, $Z_{out} = R_C = 6.8k$, $A_V = -10$

$R_E = \frac{R_C}{|A_V|} = 680\,\Omega$

$I_C = \frac{V_{CC}/2}{(R_C + R_E)} = \frac{7.5}{(\underbrace{6.8 + .68}_{7.48})} = 1mA$

$r_e = \frac{25}{I_C} = 25\,\Omega$

No "correction" to $R_E$ applied.

$V_E = R_E I_E = .68 \cdot 1 = .68\ V$ ← be warned!

$V_B = .68 + .6 = 1.28 \approx \underline{\underline{1.3V}}$

Method I: assume $\beta = 99$ → impedance looking in base

$= (\beta + 1)(r_e + R_E)$

$= 100\,(25 + 680)$

$= 70500\ \Omega$

make $R_{B1} \| R_{B2} = 7\ k\Omega$

$\frac{1.3}{15} = \frac{V_B}{V_{CC}} = \frac{R_{B1} \| R_{B2}}{R_{B2}}$

$R_{B1} = \frac{R_{B1} \| R_{B2}}{V_B / V_{CC}} = \frac{7\,k\Omega}{1.3/15} = 80.8\ k$ < 82, 75

$\frac{1}{R_{B2}} = \frac{1}{R_{B1} \| R_{B2}} - \frac{1}{R_{B1}} \Rightarrow R_{B2} = 7.6\ K$ < 7.5, 8.2

standard values

if go standard values
82, 7.5 ⇒ $V_B = 1.26$
82, 8.2 ⇒ $V_B = 1.36$

Arguments ⇒ 1.26 closer to original 1.28
→ there will be droop
→ higher temps reduces $V_{BE}$ which will increase $V_E$ → start low
→ 8.2 helps input impedance

Method 2: assume $\beta = 100 \rightarrow I_B = .01\,mA$

$$R_{B1} = \frac{(V_{cc} - V_B)}{10\, I_B} = \frac{15 - 1.3}{.1\,mA} = 137\,k\Omega \left\langle \begin{matrix} 150 \\ 130 \end{matrix} \right.$$

$$R_{B2} = \frac{(V_B - 0)}{9\, I_B} = \frac{1.3}{.09\,mA} = 14.4\,k\Omega \left\langle \begin{matrix} 15 \\ 13 \end{matrix} \right.$$

Standard values

The actual output of divider if sourcing .01 mA is almost certainly not worth the effort to calculate — but here goes

$$V_B = \frac{R_{B2}}{R_{B1} + R_{B2}} V_{cc} - (R_{B1} \| R_{B2})\, I_B = (R_{B1} \| R_{B2}) \left[ \frac{V_{cc}}{R_{B1}} - I_B \right]$$

For $\frac{130}{15} \Rightarrow 1.42$

$\frac{130}{13} \Rightarrow 1.25 \leftarrow$ if $\beta = \infty$ this goes up to 1.36

Example continued -- caps - say min freq = 100 Hz

$$\frac{1}{\omega C_{out}} \leq R_C \rightarrow \frac{1}{2\pi \cdot 100 \cdot R_C} \leq C_{out}$$

$R_C \leftarrow 6.8\,K$

$$\| \qquad .23\,\mu F$$

using $\frac{130}{13}$ basis bias circuit

$$Z_{in} = 130 \| 13 \| (\beta + 1)(\overbrace{r_e + R_E}^{705})$$

$= 11\,k\Omega$

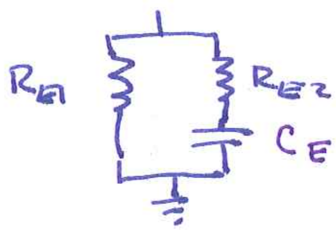
most significant part

$$\frac{1}{\omega C_{in}} \leq \frac{1}{10} Z_{in} \rightarrow \frac{10}{2\pi \cdot 100 \cdot Z_{in}} \leq C_{in}$$

$$\| \qquad 1.45\,\mu F$$

Problem: note input impedance is limited by $R_{B2}$. Additionally high gain (not that you should design for it) pushes ~~$R_E$~~ $V_E$ small - in violation of design suggestions.

Solution: push the DC level of $V_E$ up but provide a small $R_{E2}$ that the AC sees for large gain. Replace $R_E$ with below.




Design: $V_E = \frac{1}{3} V_{CC}$

$V_{CE} \approx \frac{1}{3} V_{CC}$ $= 6.8k$

$I_C = \dfrac{\frac{1}{3} V_{CC}}{R_C} \Rightarrow R_C = R_{E1}$

$R_{E2} = \dfrac{R_C}{|A_v|} = .68K$

So far only difference is $I_C = \dfrac{5V}{6.8K} = .735mA$

$r_e = 34\Omega$

Going with Method 2: $V_B = 5.6V$ $I_B = .00735mA$

$R_{B1} = \dfrac{(15 - 5.6)}{10 I_B} \approx 128K$

$R_{B2} = \dfrac{(5.6 - 0)}{9 I_B} = 85K$

AC impedance looking in base $= (\beta+1)(r_e + R_E) = 71k\Omega$ ($R_{E2}$)

$Z_{in} = 128k \| 88k \| 71k = \underline{30k}$ ← 3x better

$\dfrac{1}{\omega C_E} \le \frac{1}{10} R_{E2} \Rightarrow \dfrac{10}{2\pi \cdot 100 \cdot 680} \le 23\mu F \le C_E$

Emitter Follower – $V_{in} = V_{out}$ – $A_v = \frac{R_E}{R_E + r_e}$

NB: AC

$V_E = \frac{V_{cc}}{2} \rightarrow V_B = \frac{V_{cc}}{2} + .6$

$I_E = \frac{V_{cc}/2}{R_E} \longrightarrow I_B = \frac{1}{(\beta+1)} I_E$

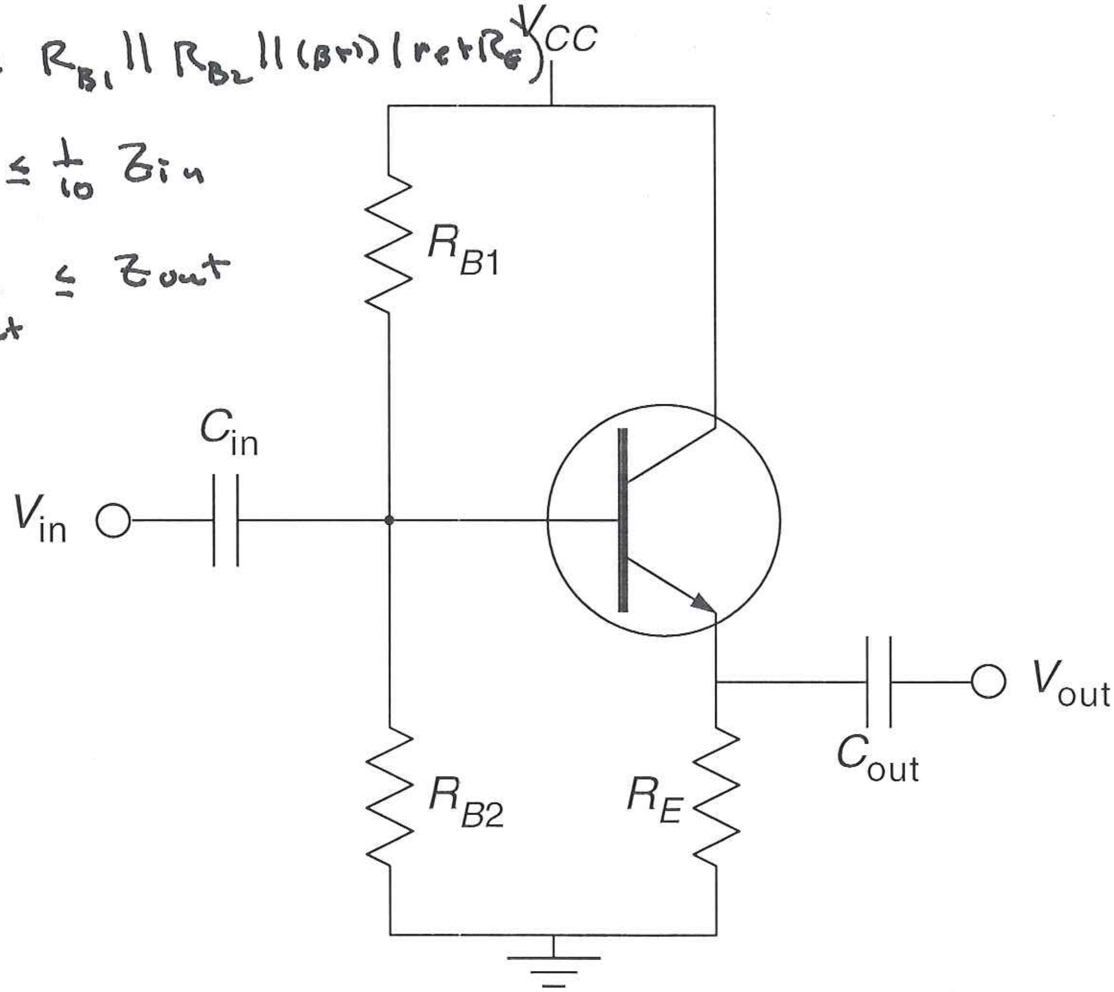
use Method 1 or Method 2 to find bias resistors

$Z_{out} = \left( \frac{R_{B1} \parallel R_{B2} \parallel R_{out}}{(\beta+1)} + r_e \right) \parallel R_E$

$Z_{in} = R_{B1} \parallel R_{B2} \parallel (\beta+1)(r_e + R_E)$

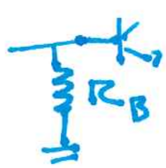
$\frac{1}{\omega C_{in}} \leq \frac{1}{10} Z_{in}$

$\frac{1}{\omega C_{out}} \leq Z_{out}$




may run this to $V_{EE}$ (say −15V)
your input signal may be around ground in which case you may not need bias resistors – IF input signal has a DC connection to ground.

IF no DC connection to ground replace $R_{B1}$ & $R_{B2}$ with




select $R_B$ to be a "shift" supply of 0 V.

Example: $V_{cc} = 15V$ ; $I_E = 1mA \Rightarrow R_E = 7.5k\Omega$

$V_E = \frac{V_{cc}}{2} = 7.5V \quad r_e = 25\Omega$

Method 1: $R_{B1} \| R_{B2} \leq \frac{1}{10}(B+1)(r_e + R_E) = 75k\Omega$

$V_B = 7.5 + .6 = 8.1$

$$\frac{V_B}{V_{cc}} = \frac{R_{B2}}{R_{B1} + R_{B2}} = \frac{R_{B1} \| R_{B2}}{R_{B1}}$$

$$R_{B1} = \frac{75k\Omega}{8.1/15} = 139k\Omega < \begin{matrix} 150 \\ 130 \end{matrix}$$ standard values

$$\frac{1}{R_{B2}} = \frac{1}{R_{B1} \| R_{B2}} - \frac{1}{R_{B1}} \Rightarrow R_{B2} = 163k\Omega < \begin{matrix} 180 \\ 160 \end{matrix}$$

(not worth calculating but below are outputs of some (some) options $R_{B1} \| R_{B2} \left( \frac{V_{cc}}{R_{B1}} - I_B \right)$

$\frac{130}{160}$ : $\rightarrow 7.56$

use these $\rightarrow$ $\frac{130}{180}$ $\rightarrow 7.95$ (unloaded: 8.71)

Method 2.

$$R_{B1} = \frac{(V_{cc} - V_B)}{10 I_B} = \frac{15 - 8.1}{.1mA} = 69k\Omega < \begin{matrix} 75 \\ 68 \end{matrix}$$

$$R_{B2} = \frac{(V_B - 0)}{9 I_B} = \frac{8.1 - 0}{.09mA} = 90k\Omega < \begin{matrix} 91 \\ 82 \end{matrix}$$ standard values

$\frac{68}{91}$ unloaded: 8.6 loaded 8.2

$Z_{in} = 130 \| 180 \| 750 = 68.6k\Omega$

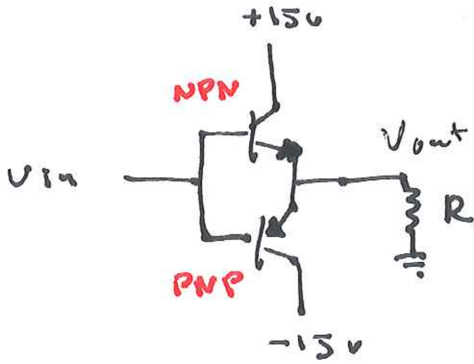
min freq = 100 $\Rightarrow$ $\frac{10}{2\pi f Z_{in}} \leq C_{in}$

$= 0.23\mu F$

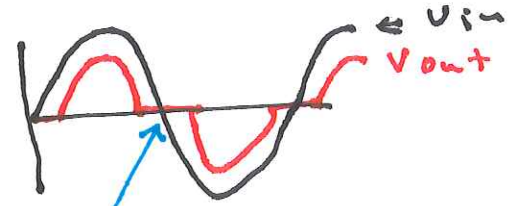
if input is wavetek with $R_{out} = 50\Omega$ $\quad Z_{out} \approx r_e = 25\Omega$

$$\frac{1}{2\pi f Z_{out}} = 64\mu F \leq C_{out}$$

push-pull emitter follower

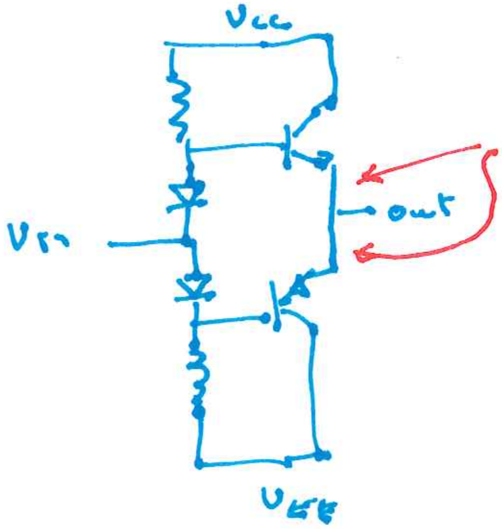



if $-.6 < V_{in} < .6$ both transistors OFF, otherwise $V_{out}$ follows $V_{in}$ $\pm .6$ diode drop




"cross over" distortion.

reduce crossover distortion




thermal changes in $V_{BE}$ - add small (1Ω) resistors and a bit more $\Delta V$ between the bases

Remark these follower stages may be driving 1 A loads. But so far we've seen mA currents. Additionally high current transistors generally have <u>reduced</u> $\beta$. "Darlington" configuration can help produce a device with $\beta^2$ effective $\beta$


one 3-terminal device with high $\beta$ effectively (but $V_{BE} = 1.2V$)