Counters

Part I

0. You investigate here two counters: the '163 (a fully synchronous, presettable binary counter) and the '191 (an up/down binary counter with asynchronous load). (Note: some protoboard 'debounced pushbuttons' will produce multiple pulses each push. If your counting seems anomalous, try clocking with the TTL function generator.)

1. Press in, and power "at the counters", the following TTL chips (from top to bottom): 74191 (up/down counter), 7400 (quad NAND), and two 74163s (counter).

2. Using the top '163, tie ENABLE T high, take ENABLE P, CLEAR, LOAD, and the data inputs D, C, B, and A to data switches and the outputs: CARRY OUTPUT, Q_D, Q_C, Q_B, and Q_A to LEDs. Begin by clocking with a NC pushbutton (remember the pull-up resistor). Note that to count, ENABLE P, CLEAR, and LOAD must all be high. Does the '163 count positive-going edges or negative-going edges? (Report your evidence!) Describe when CLEAR and LOAD need to be set and when the corresponding action occurs. Describe exactly how you would use LOAD to set the counter to 7. Carefully sketch (stacked format) the CARRY OUTPUT, CLOCK and counter value (converted to decimal) as you move towards and beyond the top count. Move the clock input from the pushbutton to the protoboard's function generator (on TTL). Set the clock rate to $\sim$1 Hz and observe the up-counting action.

3. Make a decade counter by detecting the ones in a 9-count output using a NAND and feeding the NAND output to CLEAR. Does your decade counter briefly hit 10 before clearing? Use another NAND to detect a 10 count and look for glitches with a logic probe. (Diagram how you did this!) Make 7,8,9 cycle by enabling a load of 7 following the detection of 9. Draw these circuits!

4. How can the carry be used to achieve synchronous 8-bit counting shared between two '163s? Note that using the carry as a clock to the second chip fails as the second clock tics one count too soon. (On your above stacked traces, label where such clocking would occur.) Inverting the carry would work, but would lead to a ripple counter. If two ICs are to be synchronous they must use exactly the same clock. (Hint: If the chips are clocked by the same signal, but one chip's count changes and the other's count does not, the inactive chip must be disabled.) Make a synchronous binary counter with 8 bits of output. Now make your two-163 counters have a top count of 20. Show the result to your instructor. Draw the circuit! (Your solution should be easily modifiable to make any number, e.g., 160, the top count.)

5. Investigate the behavior of the '191 as in #2. Note that LOAD must be high and ENABLE G low to count. Note that there is no CLEAR. Don't worry about the two types of carry: MAX/MIN and RIPPLE CLOCK. Describe how the up/down pin affects the counting. What sort of edge triggers the '191? What evidence shows that the '191 is asynchronous whereas the '163 is synchronous?

Part II

0. In this part you will investigate a higher level of function integration available in the 74143. This chip is a 4-bit counter, a 4-bit latch, and a seven-segment decoder/driver all in one package. This chip is designed to drive common-anode displays (N.B., *not* the common-cathode displays we used in the last lab). In a common-anode display, the high side of all the segments are internally connected together and that common-anode pin needs to be connected to +5 V. An individual segment is lit by connecting the low side of that segment "to ground." *Recall that you never actually connect a segment between ground and power as it will burn out in a quick fizzle.* The current must be somehow limited (in this case to about 15 mA). This current-limiting feature is built into the '143.

1. After removing the chips from Part I, press in (top to bottom) and power up (at the corners for the chips) a '08 (quad AND), a '143, a seven-segment display, another '143 and another display. Read the spec sheet and decide how to wire-up the various inputs so that the '143 will continuously display and count the clock input. Make a table reporting the logic level required on each input for this normal counting. Does the '143 count positive or negative edges? Note particularly the PARALLEL COUNT ENABLE INPUT, CLEAR, and the LATCH STROBE INPUT. Describe how/when each of these works. As you did for the '163, carefully sketch (stacked format) the MAX COUNT, CLOCK and counter value (converted to decimal) as you move towards and beyond the top count.

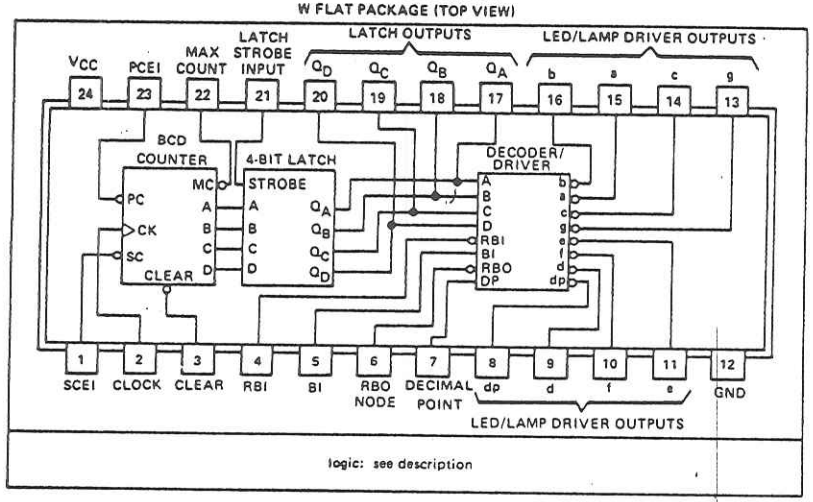
2. Figure out how you can chain your two '143s to get a two-decimal-digit count. Provide a brief circuit diagram of your solution. Is your circuit synchronous or asynchronous?

3. Make a simple stop watch using the AND as a clock gate. Wire-up CLEAR and LATCH STROBE INPUT as in a normal stop watch (i.e., include a lap-time, a reset, and start/stop options). (If you want to be fancy and include a pushbutton toggle-action start/stop, you'll need a JKFF.) Demonstrate the circuit to your instructor; write down how your circuit accomplishes these tasks (or draw the circuit).

TYPES SN54143, SN54144, SN74143, SN74144
4-BIT COUNTER/LATCH, SEVEN-SEGMENT LED/LAMP DRIVERS

BULLETIN NO. DL-S 7211538, NOVEMBER 1971—REVISED DECEMBER 1972

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



- **Choice of Driver Outputs:**

  SN54143 and SN74143 have 15-mA Constant-Current Outputs for Driving Common-Anode LED's such as TIL302 or TIL303 without Series Resistors

  SN54144 and SN74144 Drive High-Current Lamps, Numitrons†, or LED's from Saturated Open-Collector Outputs

- **Universal Logic Capabilities**

  Ripple Blanking of Extraneous Zeros
  Latch Outputs Can Drive Logic Processors Simultaneously
  Decimal Point Driver Is Included

- **Synchronous BCD Counter Capability Includes:**

  Cascadable to N-Bits
  Look-Ahead-Enable Techniques Minimize Speed Degradation When Cascaded for Large-Word Display
  Direct Clear Input

description

These TTL MSI circuits contain the equivalent of 86 gates on a single chip. Logic inputs and outputs are completely TTL/DTL compatible. The buffered inputs are implemented with relatively large resistors in series with the bases of the input transistors to lower drive-current requirements to one-half of that required for a standard Series 54/74 TTL input. The serial-count-enable, actually two internal emitters, is rated as one standard series 54/74 load. The logic outputs, except RBO, have active pull-ups.

The SN54143 and SN74143 driver outputs are designed specifically to maintain a relatively constant on-level sink current of approximately 15 milliamperes from outputs "a" through "g" and seven milliamperes from output "dp" over a voltage range from one to five volts. Any number of LED's in series may be driven as long as the output voltage rating is not exceeded.

†Trademark of RCA

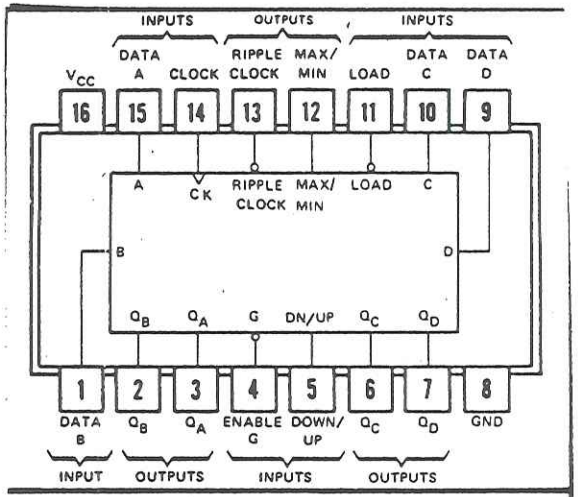
description (continued)

The SN54144 and SN74144 drivers have high-sink-current saturated outputs for driving indicators having voltage ratings up to 15 volts or requiring up to 25 milliamperes drive. The SN54144 sinks 20 milliamperes and the SN74144 sinks 25 milliamperes at an on-level voltage of 0.6 volts across their respective operating temperature ranges.

All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. Maximum clock frequency is typically 18 megahertz and power dissipation is typically 280 milliwatts. The SN54143 and SN54144 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74143 and SN74144 are characterized for operation from 0°C to 70°C.

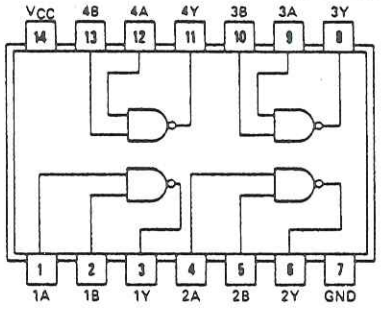
Functions of the inputs and outputs of these devices are as follows:

FUNCTION	PIN NO.	DESCRIPTION
CLEAR INPUT	3	When low, resets and holds counter at 0. Must be high for normal counting.
CLOCK INPUT	2	Each positive-going transition will increment the counter provided that the circuit is in the normal counting mode (serial and parallel count enable inputs low, clear input high).
PARALLEL COUNT ENABLE INPUT (PCEI)	23	Must be low for normal counting mode. When high, counter will be inhibited. Logic level must not be changed when the clock is low.
SERIAL COUNT ENABLE INPUT (SCEI)	1	Must be low for normal counting mode, also must be low to enable maximum count output to go low. When high, counter will be inhibited and maximum count output will be driven high. Logic level must not be changed when the clock is low.
MAXIMUM COUNT OUTPUT	22	Will go low when the counter is at 9 and serial count enable input is low. Will return high when the counter changes to 0 and will remain high during counts 1 through 8. Will remain high (inhibited) as long as serial count enable input is high.
LATCH STROBE INPUT	21	When low, data in latches follow the data in the counter. When high, the data in the latches are held constant, and the counter may be operated independently.
LATCH OUTPUTS (Q_A, Q_B, Q_C, Q_D)	17, 18, 19, 20	The BCD data that drives the decoder can be stored in the 4-bit latch and is available at these outputs for driving other logic and/or processors. The binary weights of the outputs are: $Q_A = 1$, $Q_B = 2$, $Q_C = 4$, $Q_D = 8$.
DECIMAL POINT INPUT	7	Must be high to display decimal point. The decimal point is not displayed when this input is low or when the display is blanked.
BLANKING INPUT (BI)	5	When high, will blank (turn off) the entire display and force RBO low. Must be low for normal display. May be pulsed to implement intensity control of the display.
RIPPLE-BLANKING INPUT (RBI)	4	When the data in the latches is BCD 0, a low input will blank the entire display and force the RBO low. This input has no effect if the data in the latches is other than 0.
RIPPLE-BLANKING OUTPUT (RBO)	6	Supplies ripple blanking information for the ripple blanking input of the next decade. Provides a low if BI is high, or if RBI is low and the data in the latches in BCD 0; otherwise, this output is high. This pin has a resistive pull-up circuit suitable for performing a wire-AND function with any open-collector output. Whenever this pin is low the entire display will be blanked; therefore, this pin may be used as an active-low blanking input.
LED/LAMP DRIVER OUTPUTS (a, b, c, d, e, f, g, dp)	15, 16, 14, 9 11, 10, 13, 8	Outputs for driving seven-segment LED's or lamps and their decimal points. See segment identification and resultant displays on following page.

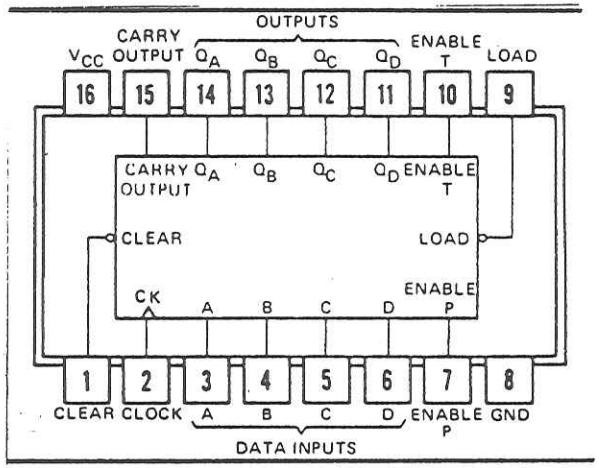


asynchronous inputs: Low input to load sets Q_A=A, Q_B = B, Q_C = C, and Q_D = D

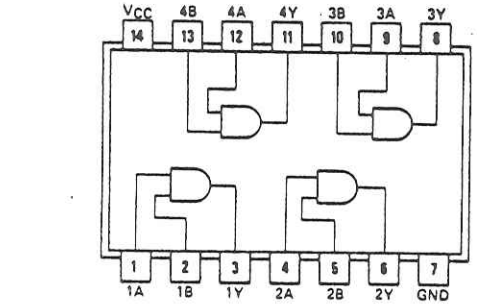
'191



'00

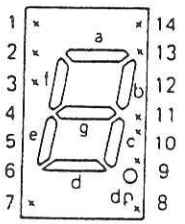


'163



'08

Pin Assignments



Pin No.	Polarity: LN514RA LN514GA LN514YA LN514OA
1	Cathode a
2	Cathode f
3	Common Anode
4	–
5	–
6	Cathode dp
7	Cathode e
8	Cathode d
9	
10	Cathode c
11	Cathode g
12	–
13	Cathod b
14	Common Anode