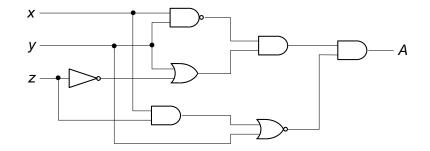
1. In the left hand side blanks "____", fill in the letter corresponding to the single best (and most specific) response.

an N-bit address selects one of 2^N out-	(a) Hi-Z state	(n) counter
puts	(b) pull-up resistor	(o) shift register
<u></u> good for serial to parallel conversion	(c) AND	(p) Bus
makes one pulse on command	(d) NAND	(q) SRFF
connects between an open collector out- put and power.	(e) NOR	(r) JKFF
effectively disconnected	(f) OR	(s) FPGA
produces a voltage proportional to an	(g) INVERTER	(t) comparator
inputted binary number	(h) BUFFER	(u) Schmitt trigger
>-	(i) wired OR	(v) monostable
V_{in} V_{out}	(j) decoder	(w) 555 timer
	(k) encoder	(x) VCO
	(l) multiplexer	(y) DAC
	(m) demultiplexer	(z) ADC

- 2. You have been asked to design the control circuitry for an automatic window shade raising/lowering system. In responding to conditions, the shade rises if up-motor control U=1 or falls if down-motor control D=1. It will remain stationary if U=0 and D=0. (U=1 and D=1should never occur.) Your circuit should monitor four boolean conditions: room temperature (H=1 is too hot), outside light (L=1 is bright sunshine), whether the shade is already at the top (if T=1) and whether the shade is already at the bottom (if B=1). The up (down) motors should not run if the shade is already at the top (bottom). The state T=0 AND B=0will occur when the shade is moving. Generally the shade should be up. The exceptions are:
 - if it is too hot inside and there is bright sunshine outside;
 - if its dark outside and cool inside.

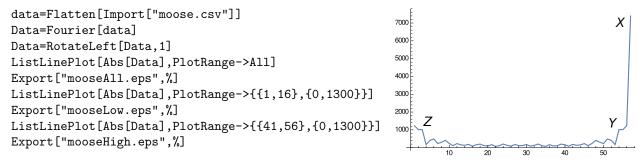
Produce a truth table for outputs U and D in terms of inputs H, L, T, B. Write a logical expression for U as a function of the inputs. Do the same for D.

- 3. Simplify the following boolean expressions:
 - (a) $x\overline{y}z + yz + \overline{x}$
 - (b) $\overline{xy + \overline{z}} + \overline{\overline{y} \cdot (\overline{x} + z)}$
 - (c) $A \overline{(CD)} + A(DB + C\overline{B})$
- 4. Consider the below mess of gates:

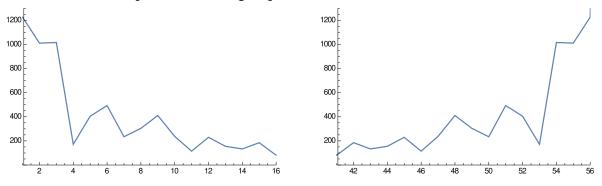


- (a) Convert the mess of gates into the equivalent boolean expression.
- (b) Use boolean algebra to reduce your boolean expression.
- (c) Directly on the above mess-of-gates circuit, label each gate with its usual name (I'm seeking a name like XOR not a number like 7486) and label the logic level of each wire for inputs: (x, y, z) = (0, 0, 0). Check that you boolean reduction matches the output you get in this part.

5. For the last 57 years researchers have reported the number of (live) moose on Isle Royale on February 15 (with the aim of looking at predator/prey relationships on an isolated island). I have performed a Fourier transform on these 57 measurements using the below code:



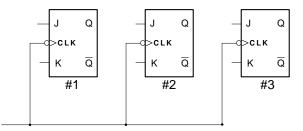
In the plot to the right of the code (mooseAll.eps) three regions have been noted: X (a single point) is the rightmost data point which is in fact the largest point and Z&Y which represent the left and right regions of the plot. These last two are displayed directly below and are mooseLow.eps and mooseHigh.eps from the above code.



- (a) Report the numerical value (with units of course): the sampling interval Δ and the Nyquist frequency.
- (b) What is represented by X? Why is it so large?
- (c) Z&Y look like mirror images of each other. Why?
- (d) Aside from X, the largest points are at 1 and 56. What frequency (with units of course) do these points represent? Points at 2 & 3 (55 & 54) are also relatively large. What period do these points represent?
- (e) The seventeen year locusts are present in large numbers every 17 years. Where (at what x-value) would such behavior show up in this plot? Some animals annually alternate population (i.e., the population each year varies as: high, low, high, low, etc.). Where would such behavior show up in this plot? Would there be any special problems associated with using the above method to measure such alternating behavior?

6. Design a synchronous circuit built from three edge-triggered JKFFs that follows the below state diagram, where the three binary digits represent the values of $Q_1Q_2Q_3$:

(i.e., the circuit cycles through the even numbers or the odd gray codes depending on the starting state). Your job is to determine the gate arrangement needed to make this cycle run, i.e., connecting the outputs of the three JKFFs: Q_i to the inputs of the three JKFFs: J_iK_i possibly using the usual (AND, OR,...) gates.



(a) Begin by considering the possible transitions of a single JKFF. What values of JK allow a particular transition? Fill in the below table. Hint: in every row either J or K will be an X for "don't care".

Transition:	J	K
$0 \longrightarrow 0$		
$0 \longrightarrow 1$		
$1 \longrightarrow 0$		
$1 \longrightarrow 1$		

(b) Now fill in the below table which displays the desired cycles

Q_1	Q_2	Q_3	J_1	K_1	J_2	K_2	J_3	K_3
0	0	0						
0	1	0						
1	0	0						
1	1	0						
0	0	1						
0	1	1						
1	1	1						
1	0	1						

- (c) Solutions for J_1 , J_3 , and K_3 can be fairly easily generated from Q_1 , Q_2 , Q_3 , HIGH, and LOW... no gates are required. What are these "easy" cases?
- (d) Solutions for K_1 , J_2 , and K_2 require a bit more work. Pick out *one* of these, K-map it, and report how it can be generated from available inputs and simple gates.